MESIONTECH

Welcome to the datasheet for our latest coprocessor! This high-performance coprocessor is designed to meet the demanding needs of XR computing applications. With advanced processing power and efficient energy usage, our coprocessor is ideal for a wide range of applications. Our chip is built with cutting-edge technology, including advanced core architecture, optimized memory bandwidth, and advanced instruction set extensions. This datasheet provides a comprehensive overview of our coprocessor's features, and technical specifications, making it the perfect resource for developers, engineers, and anyone interested in the latest developments in coprocessor technology.

A1088

Coprocessor Datasheet

V1.4

Table of Contents

1. Product Overview

A1088 is a vision positioning ASIC (Application-Specific Integrated Circuit) coprocessor with complete independent intellectual property rights. It receives data from sensors such as cameras and IMUs (Inertial Measurement Units) and, after computation and processing, outputs 6DoF (Six Degrees of Freedom) Pose information to determine the device's position and orientation. This coprocessor is primarily used as an interface and coprocessing chip for AR glasses, VR HMD (Head Mounted Device), and can also be applied to self-tracking controllers and robot vision positioning systems.

A1088, a single chip integrates complete algorithms required for visual positioning, serving as a coprocessor that conserves resources on the main chip. This reduces overall system power consumption and minimizes latency. It can be combined with low-power wearable chips or audio/video processors to design complete AR glasses and VR HMD solutions.

Application Scenarios

- AR Glasses Coprocessor
- VR Glasses Coprocessor
- Self-tracking Controller
- Robot Optical Engine Module
- Inspection and Personnel Location Terminal

Chip Capabilities

- 30 – 120FPS Visual Localization Feature Extraction
- 1000Hz 6DoF Pose Output
- MIPI IN、USB2.0/3.0 Device
- Latency < 1ms

Interface

- MIPI x 4
- USB3.0 / 2.0
- I2C x 4
- SPI x 3
- UART x 2
- PWM x 4
- GPIO x 32

Chip Packaging

- Package：FCCSP
- Dimensions：6.5×6.5 mm
- Pitch：0.4 mm

2. Specifications

MIPI	Compatible with D-PHY specification, Version 1.2 Support high-speed mode, clock, and full channel rate range of 80Mb/s to 2500Mb/s
USB	Supports USB 3.2 GEN1(maximum speed of 5Gbps/s) Supports USB2.0 low-speed, full-speed, and high-speed
I2C	I2C supports 4 channels, compatible with Philips I2C standard. Supporting three speed modes: Normal: 100Kbps, Fast: 400Kbps
SPI	3 SPI channels, compatible with Motorola SPI, TI synchronous serial, National Microwire Frame mode
QSPI	1 QPSI channel, supports memory mapping, indirect read/write mode, supports 1/2/4 IO command address read/write
UART	2 UART Interfaces
PWM	4 PWM channels
TIMER	32bit Timers for 2

3. Initialization Process

3.1 Startup Process

After firmware burning, set the BOOT pin to the boot mode (recommended ROM boot). The coprocessor will automatically power on and load the firmware program, transferring the firmware to RAM for execution.

3.2 Boot Mode

By controlling the Boot0 and Boot1 pins, you can select different boot modes for your device.

Mode		Function	Description
Boot1 (bootmode)	Boot0 (bootcfg)		
0 (Default)	0 (Default)	ROM Boot Mode (recommended)	Load firmware from ROM to RAM for execution
1	0	ROM Communication Mode	Read and write FLASH, RAM, upgrade firmware, and obtain boot version through UART
X	1	FLASH Boot Mode	Lode firmware from FLASH boot mode to RAM for execution

3.3 Flash Programming Mode

By controlling the states of the Boot0 and Boot1 pins (boot0:0, boot1:1), enter communication mode. Use an application tool to burn firmware to a specified address in Flash through the serial port.

3.4 Verified and Recommended Flash Memory

Approved Vendor List for Chip Flash Selection		
No.	Manufacturer	Part Number（2Mbit）
1	MACRONIX	MX25U2035FZUI
2	WINBOND	W25Q20EWUXIE

4. Hardware Specifications

4.1 USB3.2 GEN1 DC/AC Characteristics

Transmitter：

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
UI	Unit interval	-	199.94	200	200.06	ps
VTX-DIFF-PP	Differential peak-to-peak TX voltage swing	2 * |VTXP - VTXN|, measured at the TX near end	800	-	1200	mV
VTX-DIFF-PP_LOW	Low-power differential peak-to-peak TX voltage swing	2 * |VTXP - VTXN|, measured at the TX near end	400	-	1200	mV
VTX-DE-RATIO	TX de-emphasis level	-	3.0	-	4.0	dB
RTX-DIFF-DC	DC differential impedance	-	72	-	120	Ω
CAC-COUPLING	AC coupling capacitor	-	75	-	200	nF

Receiver：

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
UI	Unit interval	-	199.94	200	200.06	ps
RRX-DC	Receiver common-mode impedance	-	18	-	30	Ω
RRX-DIFF-DC	Receiver DC differential impedance	-	72	-	120	Ω
VRX-LFPSDET-DIFF-PP	LFPS detect threshold	-	100	-	300	mV

4.2 MIPI DC/AC Characteristics

DC in Characteristics HS Mode

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
VCMRX(DC)	Common-mode voltage in the HS receive mode	-	70	-	330	mV
VIDTH	Differential input high threshold	-	-	-	40	mV
VIDTL	Differential input low threshold	-	-40	-	-	mV
VIHHS	Single-ended input high voltage	-	-	-	460	mV
VILHS	Single-ended input low voltage	-	-40	-	-	mV
VTERM-EN	Single-ended threshold for HS termination enable	-	-	-	450	mV
ZID	Differential input impedance	-	80	100	125	Ω

AC in Characteristics HS Mode

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
ΔVCMRX(HF)	Common-mode interference beyond 450 MHz		-	-	100	mV
ΔVCMRX(LF)	Common-mode interference between 50 MHz and 450 MHz		-50	-	50	mV
CCM	Common-mode termination				60	pF

DC in Characteristics LP Mode

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
VIH	Logic 1 input voltage	-	740	-	-	mV
VIL	Logic 0 input voltage Not at the ULP state	-	-	-	550	mV
VIL-ULPS	Logic 0 input voltage At the ULP state	-	-	-	300	mV
VHYST	Input hysteresis	-	25	-	-	mV

AC in Characteristics LP Mode

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
eSPIKE	Input pulse rejection	-	-	-	300	Vps
TMIN-RX	Minimum pulse width response	-	20	-	-	ns
VINT	Peak interference amplitude	-	-	-	200	mV
fINT	Interference frequency	-	450	-	-	MHz

5. Operating Conditions

5.1 Recommended Values for the Operating Environment

Function	Min	Nom	Max	Unit
Analog USB Power Supply VCC33A_USB	2.97	3.3	3.63	V
Analog USB Power Supply VCC18A_USB	1.62	1.8	1.98	V
Analog USB Power Supply VCC09A_TX	0.81	0.9	0.99	V
Analog USB Power Supply VCC09A_RX	0.81	0.9	0.99	V
Inner Core Power supply VDD	0.81	0.9	0.99	V
Analog MIPI Power Supply VCC18A_MIPI0-3	1.62	1.8	1.98	V
Analog MIPI Power Supply VCC09A_MIPI0-3	0.81	0.9	0.99	V
Analog PLL Power Supply VDD09A_PLL	0.81	0.9	0.99	V
1.8V I/O Power Supply VDDIO	1.62	1.8	1.98	V
Operating Temperature	-10	-	55	℃
Chip Junction Temperature	-	-	125	℃

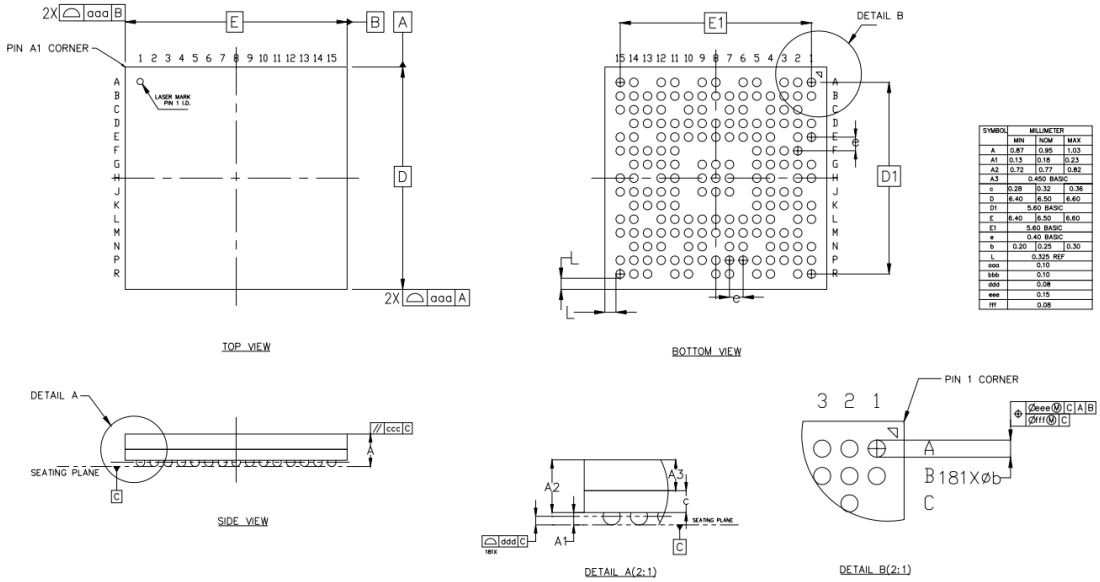
5.2 Clock Characteristics

A 30MHz external clock input from the OSC_CLK_PAD pin, powered by VDDIO.

5.3 UART Characteristics

The system or device has the capability to handle two UART (serial communication) channels. The voltage level for the UART signals is specified as 1.8V. Communication is implemented through UART0, and the default baud rate for communication mode is set to 230400.

6. Mechanical Specifications



7. I/O List

PIN Out (Top View)

No.	Location	Name	Attribute	Function
1	C6	GPIO_PAD[0]	I/O	GPIO Port
2	B5	GPIO_PAD[1]	I/O	GPIO Port
3	A5	GPIO_PAD[2]	I/O	GPIO Port
4	C4	GPIO_PAD[3]	I/O	GPIO Port
5	B4	GPIO_PAD[4]	I/O	GPIO Port
6	C7	GPIO_PAD[5]	I/O	GPIO Port
7	B3	GPIO_PAD[6]	I/O	GPIO Port
8	C3	GPIO_PAD[7]	I/O	GPIO Port
9	D5	GPIO_PAD[8]	I/O	GPIO Port
10	C2	GPIO_PAD[9]	I/O	GPIO Port
11	A3	GPIO_PAD[10]	I/O	GPIO Port
12	D4	GPIO_PAD[11]	I/O	GPIO Port
13	B2	GPIO_PAD[12]	I/O	GPIO Port
14	D6	GPIO_PAD[13]	I/O	GPIO Port
15	D3	GPIO_PAD[14]	I/O	GPIO Port
16	F2	GPIO_PAD[15]	-	Test Signal Reserved
17	A1	GPIO_PAD[16]	I/O	GPIO Port
18	B1	GPIO_PAD[17]	I/O	GPIO Port
19	G2	GPIO_PAD[18]	I/O	GPIO Port
20	E2	GPIO_PAD[19]	I/O	GPIO Port
21	G4	GPIO_PAD[20]	I/O	GPIO Port
22	E1	GPIO_PAD[21]	I/O	GPIO Port
23	D1	GPIO_PAD[22]	I/O	GPIO Port
24	F3	GPIO_PAD[23]	I/O	GPIO Port
25	H2	DBG_CLK_GPIO24_PAD	I/O	GPIO Port
26	G3	DBG_DATA0_GPIO25_PAD	I/O	GPIO Port
27	J3	DBG_DATA1_GPIO26_PAD	I/O	GPIO Port
28	H1	DBG_DATA1_GPIO27_PAD	I/O	GPIO Port
29	H4	DBG_DATA1_GPIO28_PAD	I/O	GPIO Port
30	J2	CONFIG_SPICLK_GPIO29_PAD	I/O	GPIO Port
31	G1	CONFIG_SPIDI_GPIO30_PAD	I/O	GPIO Port
32	J4	CONFIG_SPIDO_GPIO31_PAD	I/O	GPIO Port
33	K1	O_CMOSIN_DPA3_PAD	O	Test Signals Reserved
34	L1	O_CMOSIN_DNA3_PAD	O	Test Signals Reserved
35	P3	CKP[0]	I	MIPI0 Clock Signal CKP
36	P2	CKN[0]	I	MIPI0Clock Signal CKN
37	R2	DP0[0]	I	MIPI0 Data Signal DP0
38	R1	DN0[0]	I	MIPI0 Data Signal DN0
39	N3	DP1[0]	I	MIPI0 Data Signal DP1
40	N4	DN1[0]	I	MIPI0 Data Signal DN1
41	N1	DP2[0]	I	MIPI0 Data Signal DP2
42	P1	DN2[0]	I	MIPI0 Data Signal DN2
43	L2	DP3[0]	I	MIPI0 Data Signal DP3

44	M2	DN3[0]	I	MIPI0 Data Signal DN3
45	R5	CKP[1]	I	MIPI1 Clock Signal CKP
46	R4	CKN[1]	I	MIPI1 Clock Signal CKN
47	R8	DP0[1]	I	MIPI1 Data Signal DP0
48	R7	DN0[1]	I	MIPI1 Data Signal DN0
49	P6	DP1[1]	I	MIPI1 Data Signal DP1
50	P7	DN1[1]	I	MIPI1 Data Signal DN1
51	P9	CKP[2]	I	MIPI2 Clock Signal CKP
52	P10	CKN[2]	I	MIPI2 Clock Signal CKN
53	P12	DP0[2]	I	MIPI2 Data Signal DP0
54	P11	DN0[2]	I	MIPI2 Data Signal DN0
55	R11	DP1[2]	I	MIPI2 Data Signal DP1
56	R10	DN1[2]	I	MIPI2 Data Signal DN1
57	R14	CKP[3]	I	MIPI3 Clock Signal CKP
58	R13	CKN[3]	I	MIPI3 Clock Signal CKN
59	N14	DP0[3]	I	MIPI3 Data Signal DP0
60	P14	DN0[3]	I	MIPI3 Data Signal DN0
61	P15	DP1[3]	I	MIPI3 Data Signal DP1
62	R15	DN1[3]	I	MIPI3 Data Signal DN1
63	M4	RBIAS[0]	I/O	MIPI0 Bias Voltage
64	M5	RBIAS[1]	I/O	MIPI1 Bias Voltage
65	N6	RBIAS[2]	I/O	MIPI2 Bias Voltage
66	M7	RBIAS[3]	I/O	MIPI3 Bias Voltage
67	M13	SPI_NSS_0_PAD	O	SPI0 Slave Select Signal
68	M12	SPI_SCK_0_PAD	O	SPI0 Clock signal
69	M15	SPI_MOSI_0_PAD	O	SPI0 MOSI Signal
70	N12	SPI_MISO_0_PAD	I	SPI0 MISO Signal
71	A6	SPI_NSS_1_PAD	O	SPI1 Slave Select Signal
72	B6	SPI_SCK_1_PAD	O	SPI1 Clock Signal
73	B7	SPI_MOSI_1_PAD	O	SPI1 MOSI Signal
74	B8	SPI_MISO_1_PAD	I	SPI1 MISO Signal
75	F4	SPI_NSS_2_PAD	O	SPI2 Slave Select Signal
76	E4	SPI_SCK_2_PAD	O	SPI2 Clock Signal
77	A2	SPI_MOSI_2_PAD	O	SPI2 MOSI Signal
78	D2	SPI_MISO_2_PAD	I	SPI2 MISO Signal
79	C13	FLASH_SS_0_PAD	O	QSPI Slave Select signal 0
80	D9	FLASH_SS_1_PAD	O	QSPI Slave Select Signal 1
81	C9	FLASH_SS_2_PAD	O	QSPI Slave Select Signal 2
82	B14	FLASH_SS_3_PAD	O	QSPI Slave Select Signal 3
83	D12	FLASH_MIO_0_PAD	I/O	QSPI MIO0 Signal
84	D13	FLASH_MIO_1_PAD	I/O	QSPI MIO1 Signal
85	D10	FLASH_MIO_2_PAD	I/O	QSPI MIO2 Signal
86	D11	FLASH_MIO_3_PAD	I/O	QSPI MIO3 Signal
87	F11	FLASH_SCLK_PAD	O	QSPI Clock Signal
88	A12	SSTXA	O	USB3.0 TX+
89	A11	SSTXB	O	USB3.0 TX-
90	A15	SSRXA	I	USB3.0 RX+
91	A14	SSRXB	I	USB3.0 RX-

92	A8	DP	I/O	USB2.0 D+
93	A9	DM	I/O	USB2.0 D-
94	B10	RREF	I/O	USB Bias Voltage
95	G12	UART_TXD_PAD	O	UART TXD Signal
96	D14	UART_RXD_PAD	I	UART RXD Signal
97	C15	UART1_TXD_PAD	O	UART1 TXD Signal
98	C14	UART1_RXD_PAD	I	UART1 RXD Signal
99	H15	I2C_SCL_0_PAD	O	I2C0 Clock Signal
100	F15	I2C_SDA_0_PAD	I/O	I2C0 Data Signal
101	J12	I2C_SCL_1_PAD	O	I2C1 Clock Signal
102	G13	I2C_SDA_1_PAD	I/O	I2C1 Data Signal
103	J13	I2C_SCL_2_PAD	O	I2C2 Clock Signal
104	G14	I2C_SDA_2_PAD	I/O	I2C2 Data Signal
105	F14	I2C_SCL_3_PAD	O	I2C3 Clock signal
106	H12	I2C_SDA_3_PAD	I/O	I2C3 Data Signal
107	L15	PWM_OUT_CAM0_PAD	O	PWM0 Output Signal
108	N9	PWM_OUT_CAM1_PAD	O	PWM1 Output Signal
109	M8	PWM_OUT_CAM2_PAD	O	PWM2 Output Signal
110	M14	PWM_OUT_CAM3_PAD	O	PWM3 Output Signal
111	B13	I_ISOEN_PAD	I	Reserved Test Signal
112	C10	I_BOOTCFG_PAD	I	BOOT Configuration
113	B9	I_BOOTMODE_PAD	I	BOOT Mode
114	B11	I_REMAP_PAD	I	Test Signal Reserved
115	C12	I_BPOCC_PAD	I	Test Signal Reserved
116	K12	TEST_EN_PAD	I	Test Mode Enable Signal
117	J15	TEST_MODE_PAD[0]	I	Test Signal Reserved
118	K13	TEST_MODE_PAD[1]	I	Test Signal Reserved
119	H14	TEST_RSTN_PAD	I	Test Mode Reset signal
120	B12	NA1	-	Test Signal Reserved
121	E12	NA2	-	Test Signal Reserved
122	F12	NA3	-	Test Signal Reserved
123	B15	NA4	-	Test Signal Reserved
124	F13	NA5	-	Test Signal Reserved
125	L14	O_CAM0CLK_PAD	O	Clock Output Signal
126	J14	O_CAM1CLK_PAD	O	Clock Output Signal
127	N10	GLASS_VSYNC_PAD	I	Display Sync signal
128	E14	GLOBAL_RSTN_PAD	I	Reset Signal
129	E15	OSC_CLK_PAD	I	Clock Input Signal
130	M3	VCC09A_MIPI0	PWR	MIPI0 Analog Voltage Power Supply
131	K4	VCC18A_MIPI0	PWR	MIPI0 Analog Voltage Power Supply
132	K3	VCC12A_MIPI0	PWR	MIPI0 Calibration Voltage
133	P5	VCC09A_MIPI1	PWR	MIPI1 Analog Voltage Power Supply
134	L6	VCC18A_MIPI1	PWR	MIPI1 Analog Voltage Power Supply
135	L4	VCC12A_MIPI1	PWR	MIPI1 Calibration Voltage

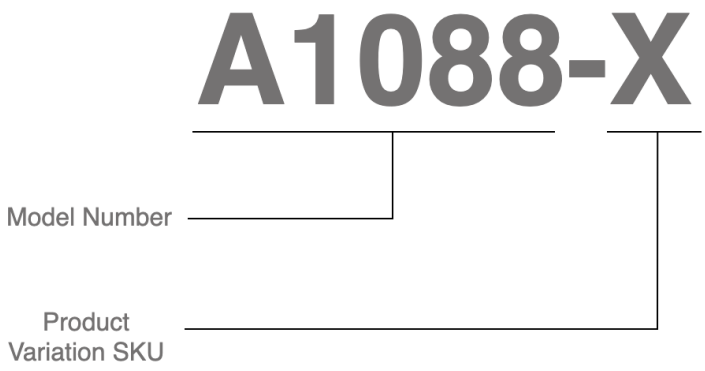
136	N7	VCC09A_MIPI2	PWR	MIPI2 Analog Voltage Power Supply
137	L7	VCC18A_MIPI2	PWR	MIPI2 Analog Voltage Power Supply
138	M6	VCC12A_MIPI2	PWR	MIPI2 Calibration Voltage
139	N13	VCC09A_MIPI3	PWR	MIPI3 Analog Voltage Power Supply
140	L8	VCC18A_MIPI3	PWR	MIPI3 Analog Voltage Power Supply
141	M9	VCC12A_MIPI3	PWR	MIPI3 Calibration Voltage
142	N2	GND09A_MIPI0	PWR	MIPI0 Analog Ground
143	P4	GND09A_MIPI1	PWR	MIPI1 Analog Ground
144	P8	GND09A_MIPI2	PWR	MIPI2 Analog Ground
145	P13	GND09A_MIPI3	PWR	MIPI3 Analog Ground
146	E9	VCC09A_TX	PWR	USB Analog Voltage Power Supply
147	E11	VCC09A_RX	PWR	USB Analog Voltage Power Supply
148	E7	VCC18A_USB	PWR	USB Analog Voltage Power Supply
149	D8	VCC33A_USB	PWR	USB Analog Voltage Power Supply
150	E6	GNA_USB	PWR	USB Analog Ground
151	D7	GNA_USB	PWR	USB Analog Ground
152	E10	GNA_USB	PWR	USB Analog Ground
153	E8	GNA_USB	PWR	USB Analog Ground
154	K14	VBUS_PAD	PWR	USB Vbus Power detection
155	M11	VDD09A_PLL	PWR	PLL Analog Voltage Power Supply
156	M10	VSS09A_PLL	PWR	PLL Analog Ground
157	L12	VQPS	PWR	eFuse Programming Voltage Power Supply
158	F5	VDDIO	PWR	GPIO Power Supply Port
159	G5	VDDIO	PWR	GPIO Power Supply Port
160	L9	VDDIO	PWR	GPIO Power Supply Port
161	L10	VDDIO	PWR	GPIO Power Supply Port
162	E5	VSSIO	PWR	GPIO Digital Ground Port
163	G11	VSSIO	PWR	GPIO Digital Ground Port
164	H11	VDD	PWR	0.9V Digital Voltage Power Supply
165	J11	VDD	PWR	0.9V Digital Voltage Power Supply
166	K11	VDD	PWR	0.9V Digital Voltage Power Supply
167	L11	VDD	PWR	0.9V Digital Voltage Power Supply
168	H5	VDD	PWR	0.9V Digital Voltage Power Supply
169	J5	VDD	PWR	0.9V Digital Voltage Power Supply
170	K5	VDD	PWR	0.9V Digital Voltage Power Supply

171	L5	VDD	PWR	0.9V Digital Voltage Power Supply
172	K2	VSS	PWR	Connect PCB GND
173	G7	VSS	PWR	Connect PCB GND
174	H7	VSS	PWR	Connect PCB GND
175	J7	VSS	PWR	Connect PCB GND
176	G8	VSS	PWR	Connect PCB GND
177	H8	VSS	PWR	Connect PCB GND
178	J8	VSS	PWR	Connect PCB GND
179	G9	VSS	PWR	Connect PCB GND
180	H9	VSS	PWR	Connect PCB GND
181	J9	VSS	PWR	Connect PCB GND

8. Ordering Information

Part Number	Package	Operating Temperature	MSL	Packing Method
A1088 A1088-D A1088-M	FCCSP 6.5X6.5mm	Commercial -10°C to +55°C	3	Tray Packing • 1 Tray=260 pcs • MPQ=2,600 pcs (10 Trays Sealed in 1 Vacuum Bag) • 1 Carton=15,600 pcs (6 Packs of Vacuum Bags) Reel Packing • 1 Reel=3,000 pcs • MPQ=3,000 pcs (1 Reel Pack with Seal Vacuum Bag) • 1 Carton=24,000 pcs (8 Packs of Vacuum Bags)

9. Product Model Number



A1088 = AR/VR/MR Categories
A1088-D = XR Controllers / Optical Engine Module / Service Robots / Drones
A1088-M = Microcontroller Unit

10. Document Version

Version	Date	Changes
1.0	2023/12/10	Production release

1.1	2024/2/29	Update I/O List for MIPI Out to MIPI In item number from 35 to 62 Update I/O List for I2C Clock Signal in item number from 99 to 106
1.2	2024/9/3	Update I/O List for Test Signal Reserved in item number of 16
1.3	2024/10/14	Update product model number
1.4	2025/2/8	Add reel packing method for production purpose